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Signal Integrity Series:

Shortening the Development Cycle with Effective Eye Measurements

April 16, 2002

presented by:

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What this eSeminar will cover

- Eye measurement basics
- Eye measurements in the development cycle
  - Eye measurements in design
  - Eye measurements in validation
- Eye measurement tools
- Additional resources

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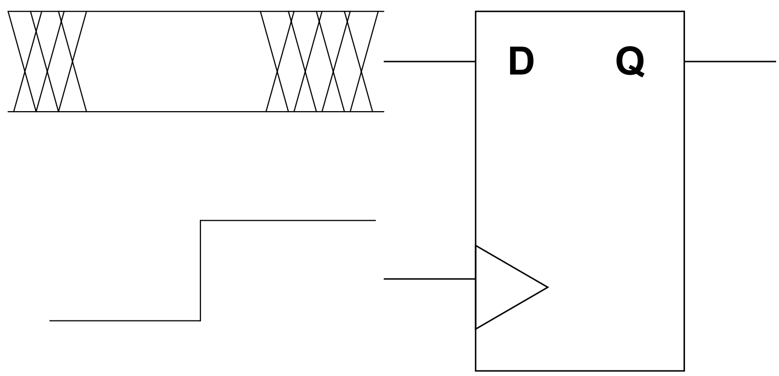
Today I'm going to discuss one of the most useful and comprehensive measurements in the signal integrity arena – eye diagrams. You can save a significant amount of time by using eye measurements effectively. In this eSeminar you will learn what information is visible in an eye diagram, how eye diagrams can help you in achieving your signal integrity goals, where eye diagrams play a role in the design cycle, what tools are available from Agilent and Agilent's partners for eye diagram measurements, and what to look for in choosing equipment for eye diagram measurements. I'll cover the basics of eye diagrams, then talk about where eye diagrams fit in the development cycle. The meat in today's sandwich is "live" eye diagram measurements, but I want to spend a little time also talking about eye diagrams in the design phase of development.

Synchronous logic



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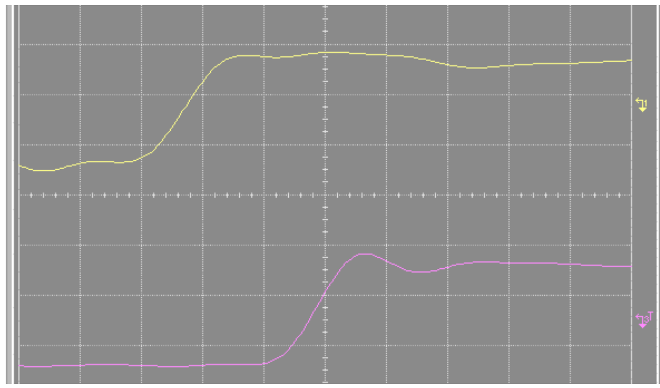
First, what is an eye diagram? [Explain how the eye is derived, talk about clock and data]

Building the eye

Data

Clock



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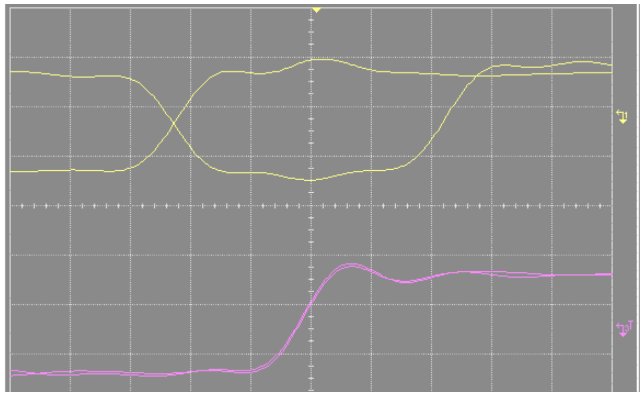
Building the eye

Data

Clock



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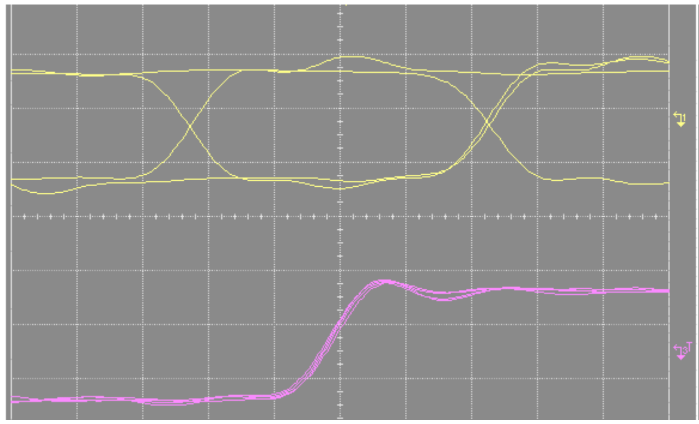
Building the eye

Data

Clock



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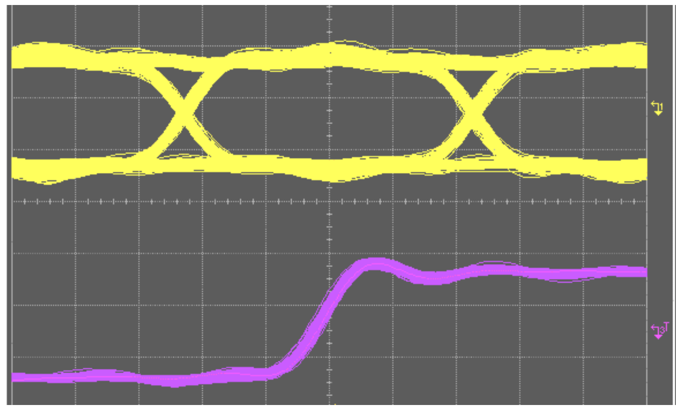
Building the eye

Data

Clock



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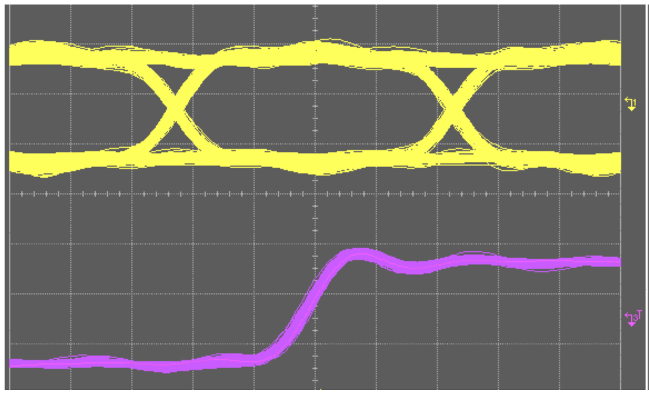
Basics

Why is an eye diagram valuable?



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The eye diagram is valuable because…

Basics

Why is an eye diagram valuable?

Comprehensive view of all signal integrity faults (except clock jitter)

- **Noise**
- **Jitter**
- **Reflections**
- **Ringing**
- **Intersymbol interference**
- **Power and ground coupling**

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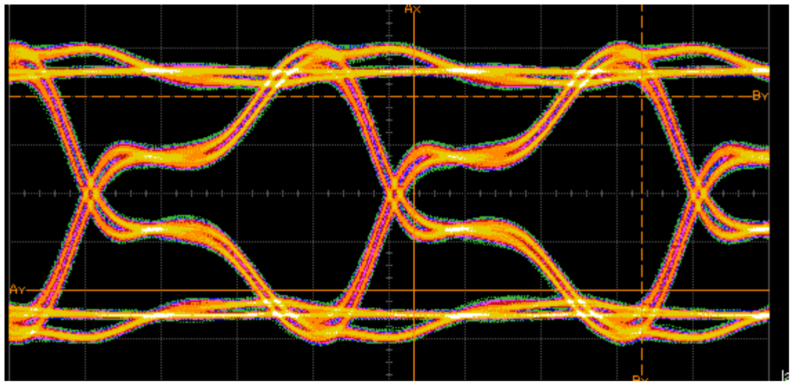
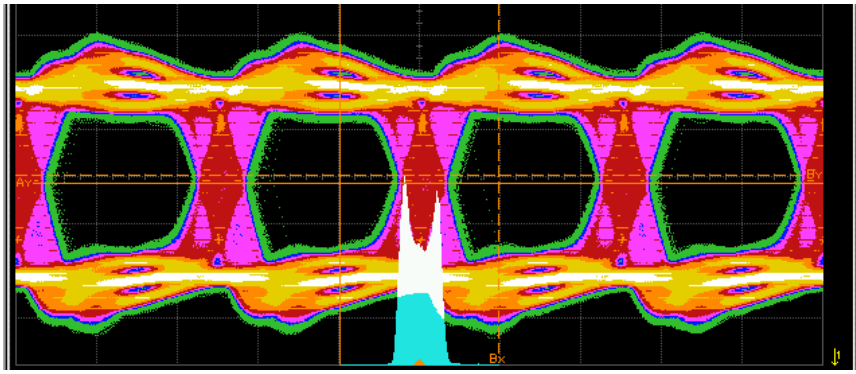
It gives you a comprehensive overview of all the factors that contribute to timing and signal integrity problems. Noise, jitter, reflections, ringing, intersymbol interference, pattern-dependent delay jitter, the effects of all these and more will be visible in the eye diagram. So it's a great way to get a quick, first view to determine if you have any signal integrity problems. If you don't, you can check that box and go on to the next task.

Bad termination



Jitter



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What an eye diagram doesn't tell you

- Clock jitter
- Bit error rate

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However, an eye diagram does not reveal everything that could cause you problems. In the eye you see data jitter relative to the clock on every individual cycle, but you won't see jitter in the clock. That's because the clock sets the time reference for the eye measurement.

The eye measurement also won't directly predict the bit error rate. The eye will show what the receiver sees, but it doesn't tell you what the receiver's "real" timing and noise margins are. Data valid window, setup and hold, and noise margin, which you can examine in the eye diagram, are designed to form a contract between the receiver designer and the system designer. In general,what you can say is, the smaller the eye, the higher the probability of errors. However, if the eye is much larger than the receiver's margins, so there is plenty of margin, small changes in the size of the eye don't necessarily translate to changes in bit error rate.

The message here is, it's usually a good idea to allow for some additional margin in the eye.

We'll talk later about an instrument that does in fact derive an eye from isocontour plots of bit error rate; in that case there is a direct relationship between the eye diagram and the bit error rate.

What this eSeminar won't cover

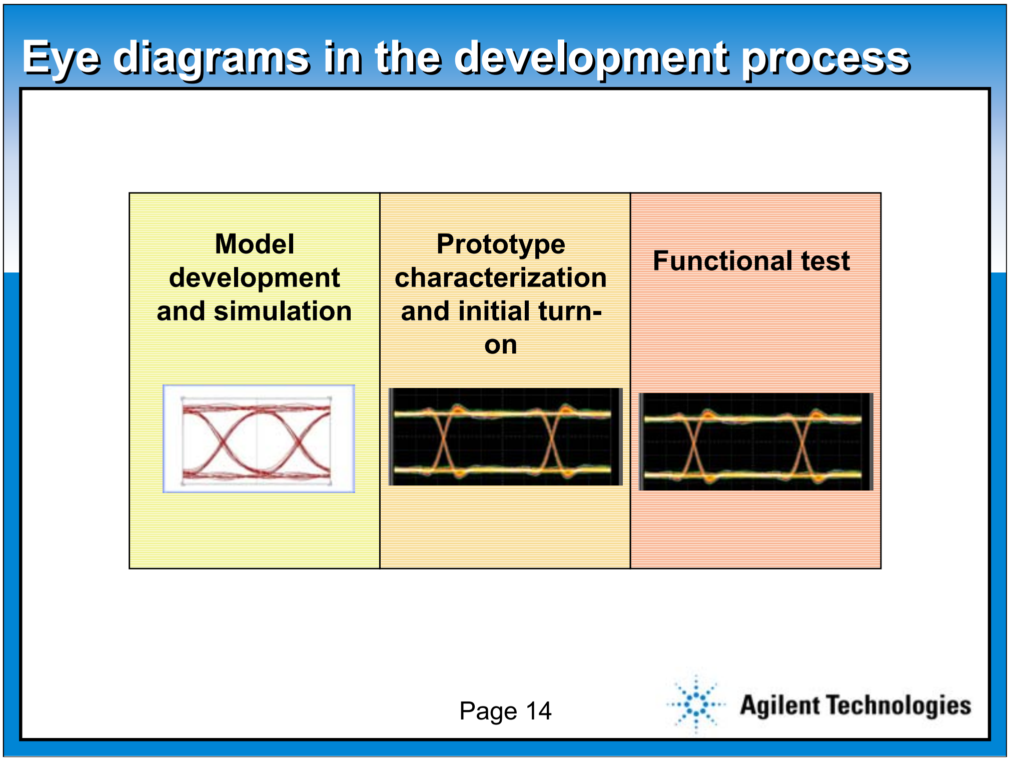
- Optical measurements
- RF measurements
- Box-to-box measurements
- Manufacturing test

In this eSeminar, I will be focusing on electrical measurements on traces running between components on PC boards. Most of the topics and principles I'll cover are generally applicable, but I won't spend any time talking about optical measurements, RF measurements, or cable measurements. Also I won't be covering some of the specific eye measurements that are common in communication standards.

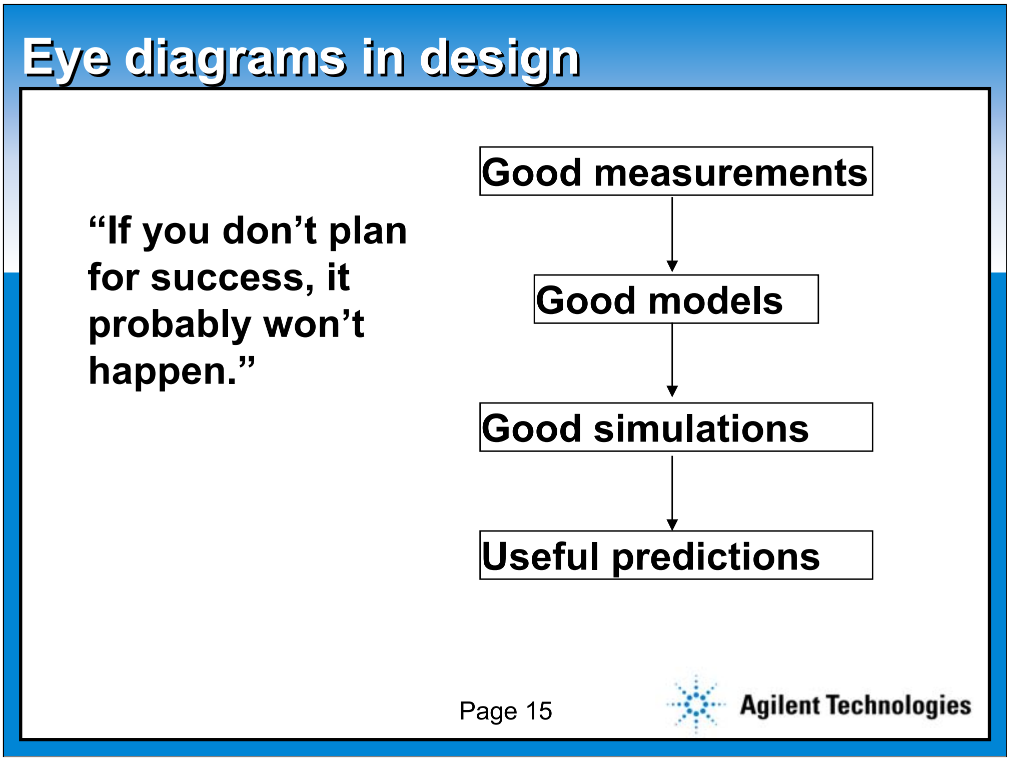
I'll be focusing on R&D in this eSeminar. Again, most of the content is widely applicable, but I won't be specifically dealing with the issues of eye measurements in manufacturing or field test.

By the way, don't expect a 90-minute condensation of a semester-long course today. This will be a pretty high-level overview of the topic. You turn me loose, I could talk for weeks about eye measurements, but we've only got an hour.

Also this won't be step-by-step how-to tutorial on how to set up a specific instrument to make an eye measurement on a specific device under test.



Eye measurements are used in every phase of development.

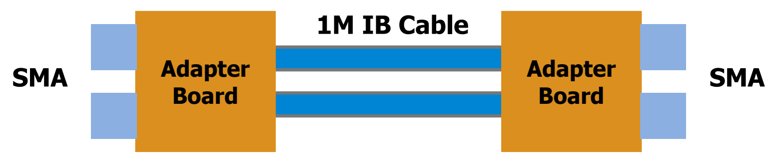


The key to success is to be thinking about success at every stage, from when you first start the project. Defining your signal integrity goals is as critical as any other requirement.

If you have a set of goals in mind, then you can check at each stage to see if you're meeting them. That way, you find problems as early in the development cycle as possible. The earlier you find them, the earlier you can fix them.

The key to useful eye diagram predictions is to start with good measurements. You can't have good models without good measurements. I think Eric stressed this sufficiently in his eSeminar, but I want to stress it again here. I don't want you to wait until you get your first board and silicon back, then find out you have signal integrity problems, only to find that it all started with bogus TDR or VNA measurements. By the way, that is the topic of the next eSeminar in this series.

Example: InfiniBand patch cable



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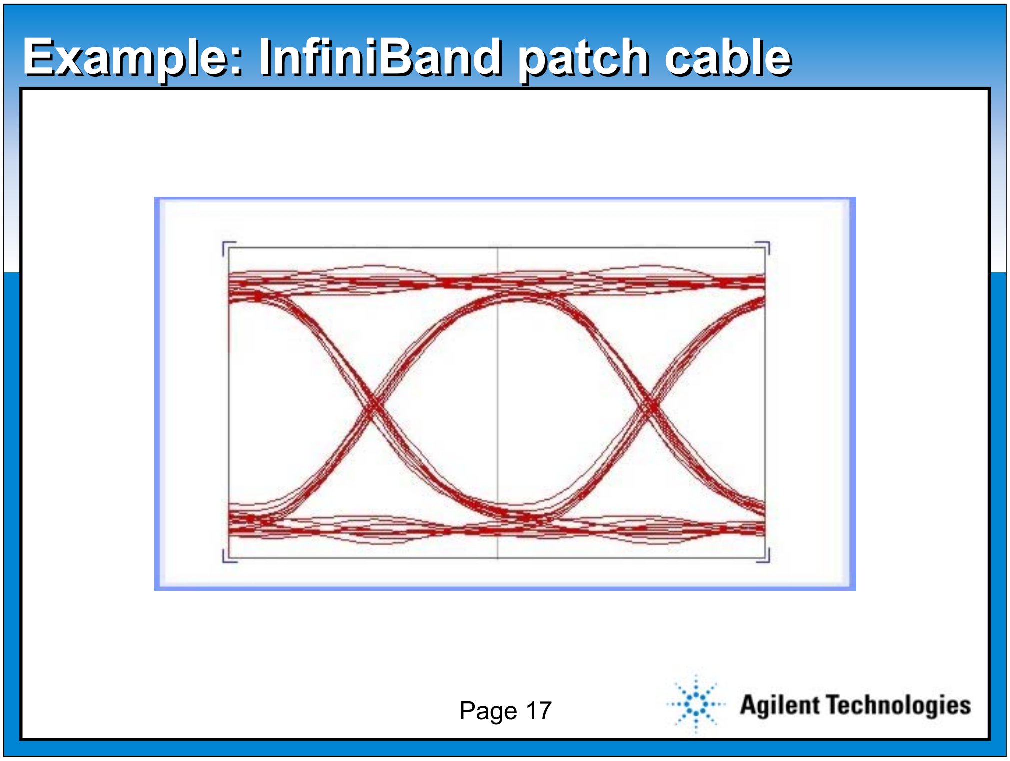
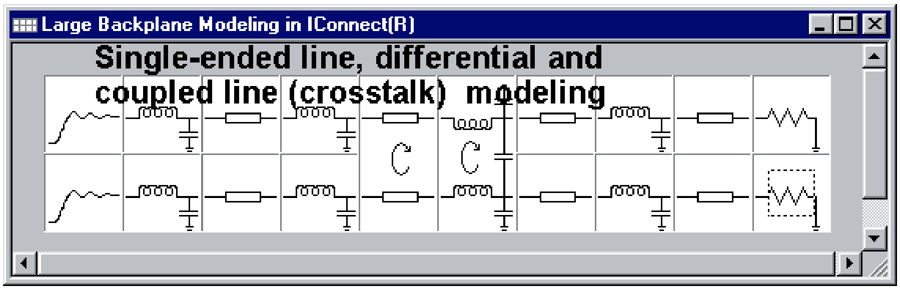
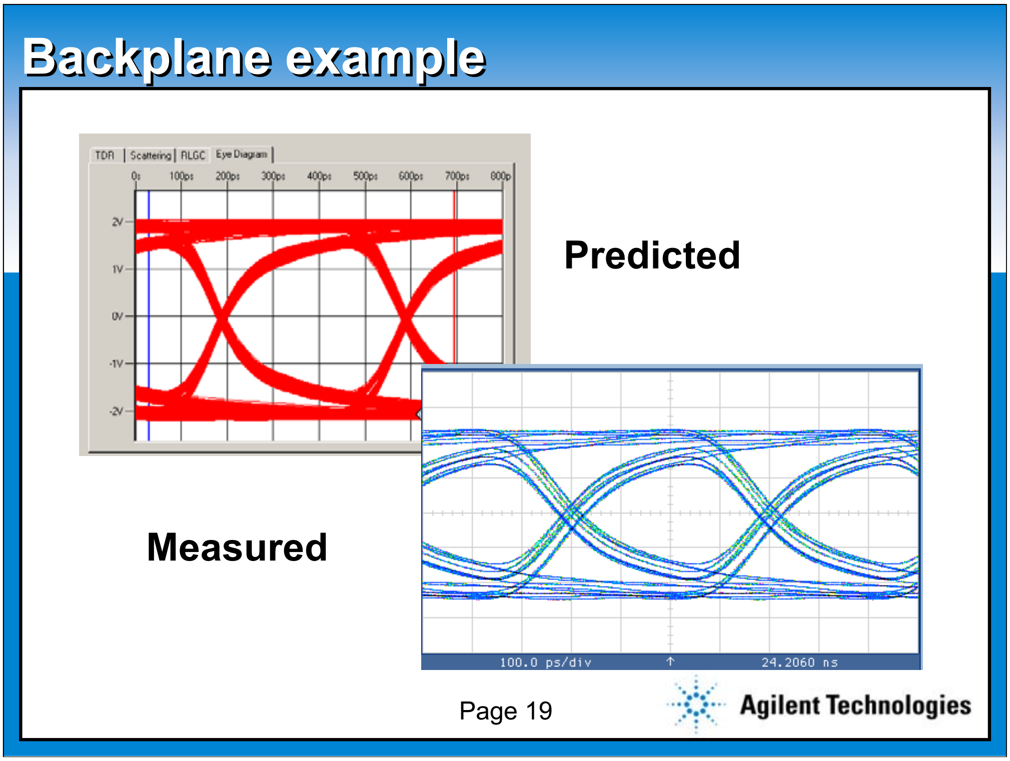


This is an example of a 1 meter Infiniband patch cable design. (There I go already, I said I wouldn't talk about cables, and here in my first example I am talking about a cable.) This was generated from a model that was developed from VNA (vector network analyzer) measurements of the cable. The designer tried out various terminations for the cable until the optimum termination was determined by the simulation.

Backplane example



In the next example, time domain reflectometry (TDR) was used to develop and validate the model of a backplane. Simulations were then made using these models to predict the eye opening.



You can see good agreement between the simulated and measured eye diagram.

Eye diagrams in validation

- Stimulus-response measurements
- Circuit runs on its own (autonomous)

So, let's leave the design phase now (don't you wish it went that fast on real projects?) and move on to real circuits. You got your first prototype back, now you need to make some real-world eye measurements.

Those take 2 flavors, which are worth distinguishing because the tools you use and the best practices are different in some ways.

Key factors for success: stimulus-response

- Time-domain characteristics of stimulus and response measuring instruments
  - Flatness
  - Rise and fall times
  - Stability
- Connections and probing

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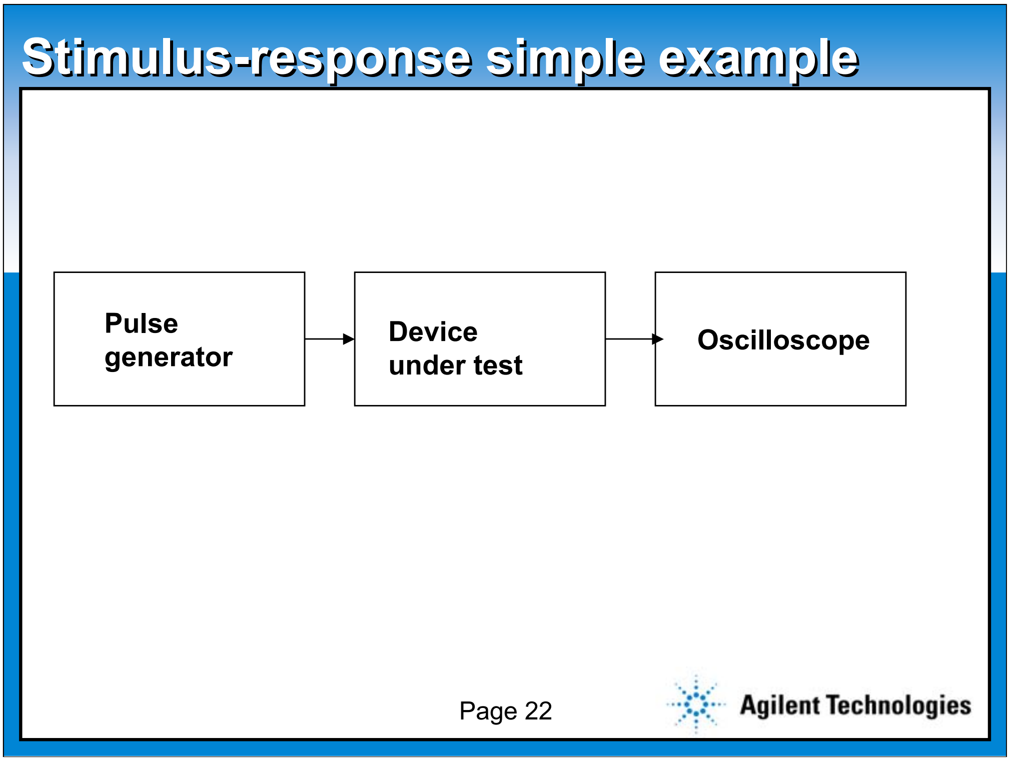
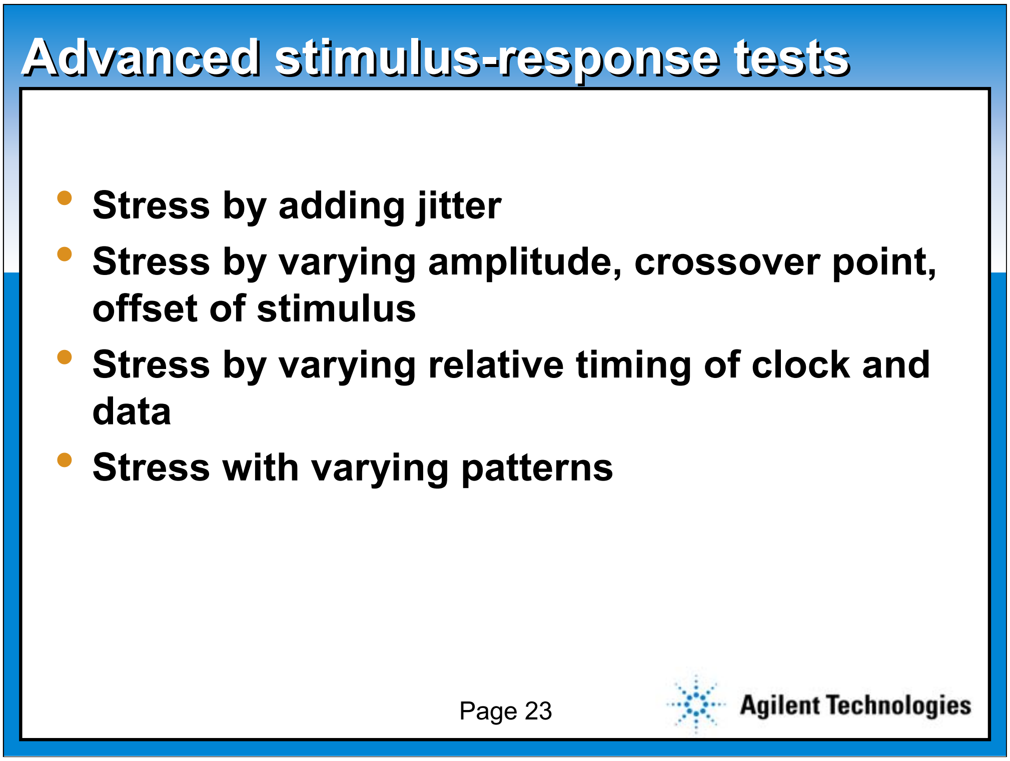
First let's discuss stimulus-response measurements, in which you provide the gozinta and observe the gozoutta. The device under test can be active or passive, linear or nonlinear, simple or complex.

Key factors for success here are the time domain characteristics of the stimulus and response instruments, and the connections to the device under test. Many a bad measurement has been made with good instruments by not paying attention to the connections. Remember, the input and output connections are part of the test. We'll talk more about that as we go along.



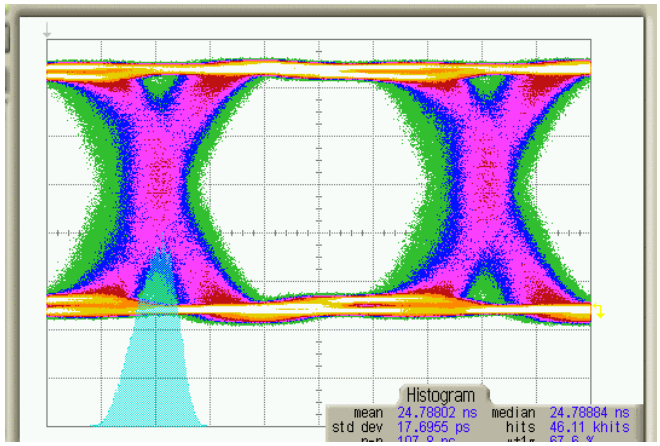
The simplest example of a stimulus-response test is a pulse generator driving an input to a device under test, and a scope measuring the output.



While you're at it, you might as well get all the information you can out of the measurement by stressing the device under test to determine its operating margins. In addition to varying the power supply voltage and operating temperature, you can stress it further by adding jitter to the incoming signals, by varying the amplitude and offset of the stimulus (and the crossover point, if it's differential), and by varying the timing.

It is very important to be able to generate serial patterns such as pseudorandom binary sequence (PRBS), so you can detect pattern-dependent delay and ISI (intersymbol interference), which can lead to unanticipated jitter.

Adding known jitter



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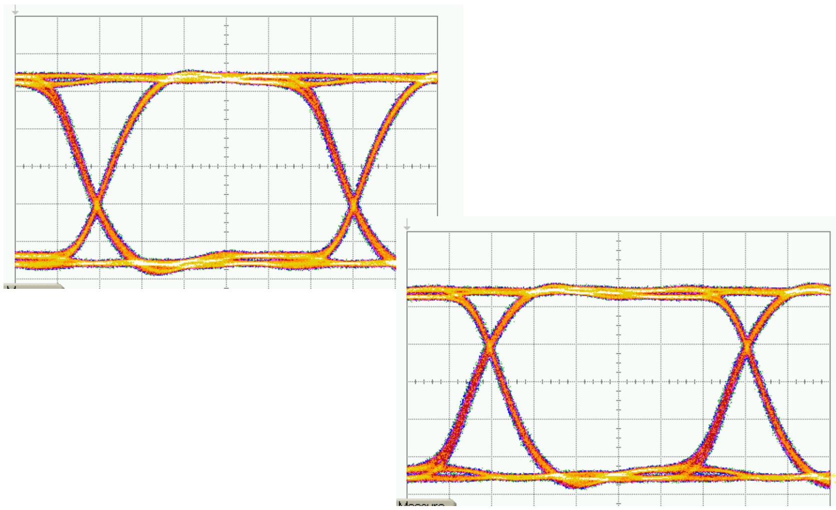
Here is an example of adding jitter to the stimulus, using a pulse generator with the ability to modulate the period.

Varying crossover point



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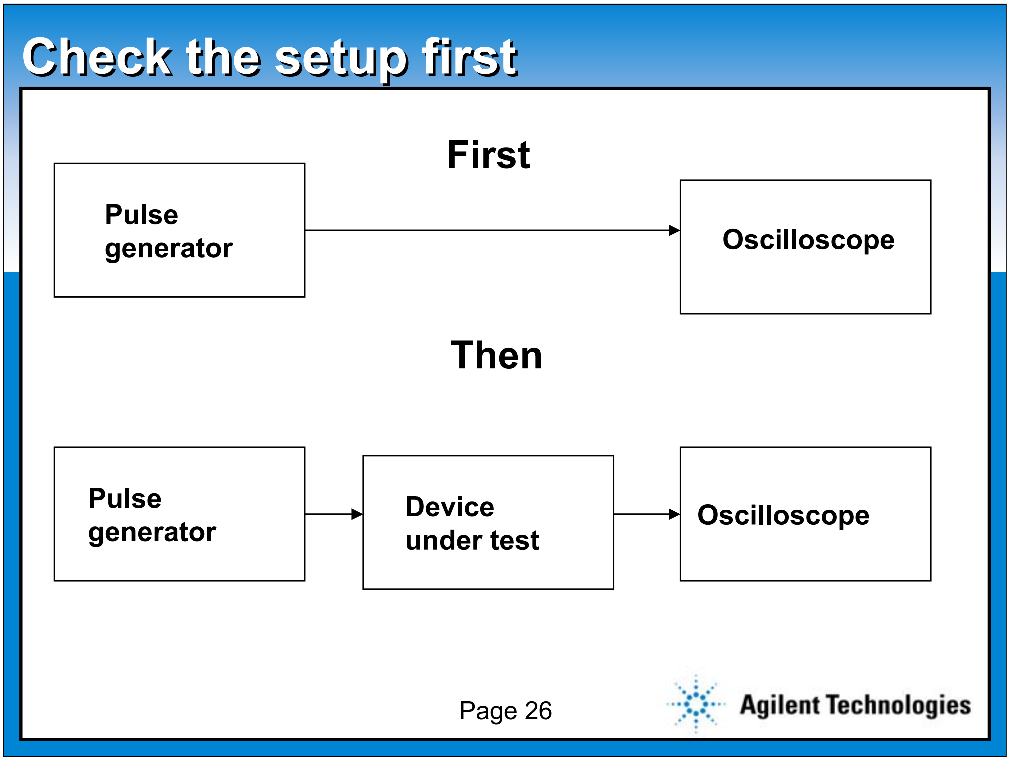
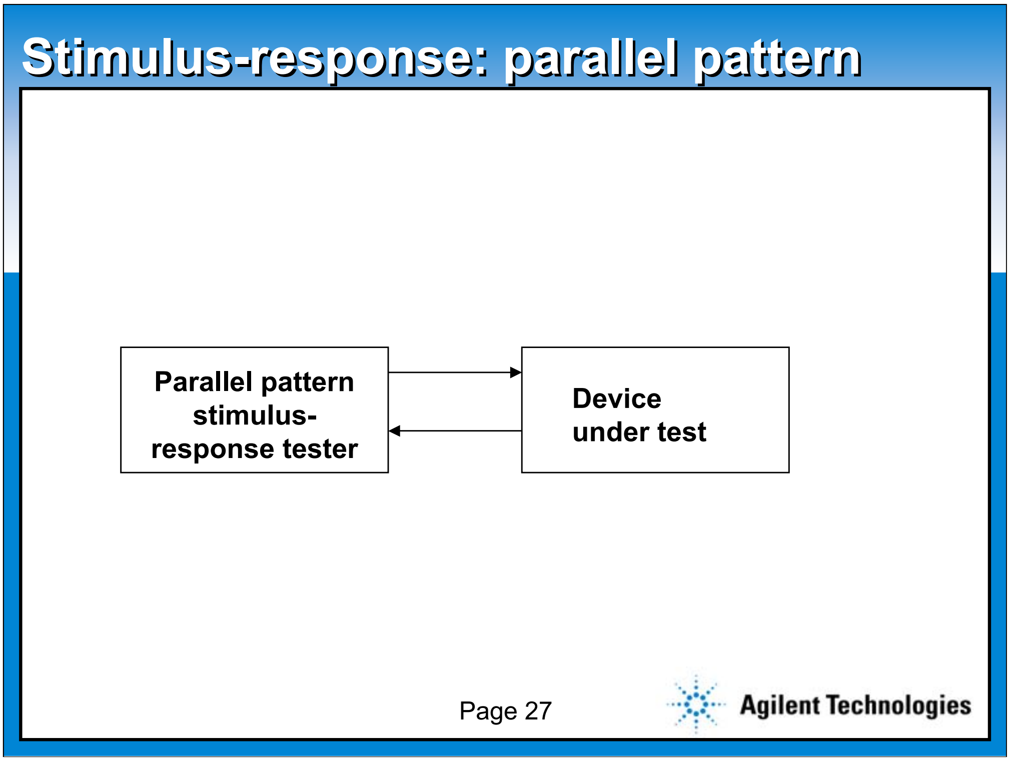
With some generators you can also vary the crossover point of differential signals. Assume your real circuit won't always get ideal signals from the device that is driving it.

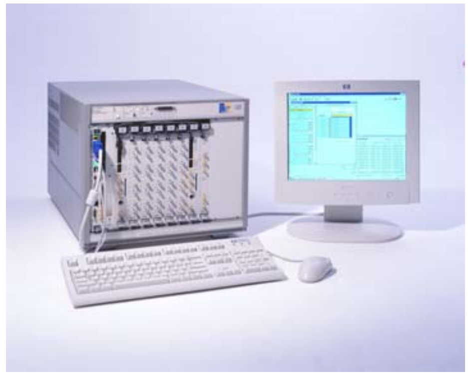


The key to dependable stimulus-response measurements is to check out the test equipment and the connections first. The simplest way to do that is to remove the device under test from the measurement. If you don't see a good eye with the device removed, you probably won't see a good eye with the device inserted.



Another flavor of stimulus-response testing: Using an instrument that both provides the stimulus and analyzes the response. This also illustrates using a parallel pattern, as opposed to just one wire.

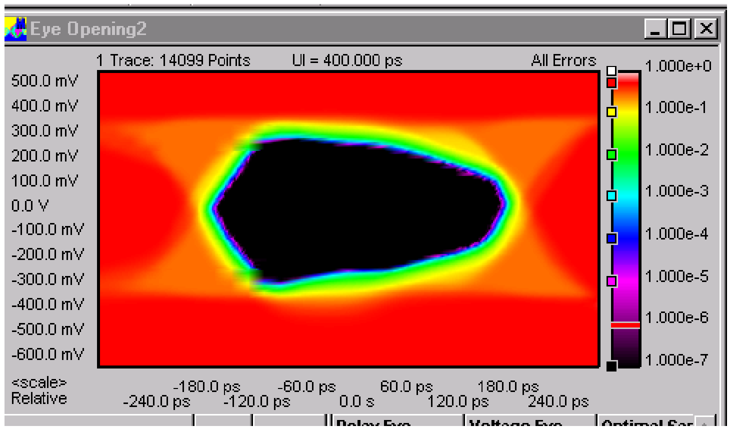
Parallel pattern test



Parallel-pattern stimulus-response tester

Here is an instrument of that type.

BER Eye Opening Measurement



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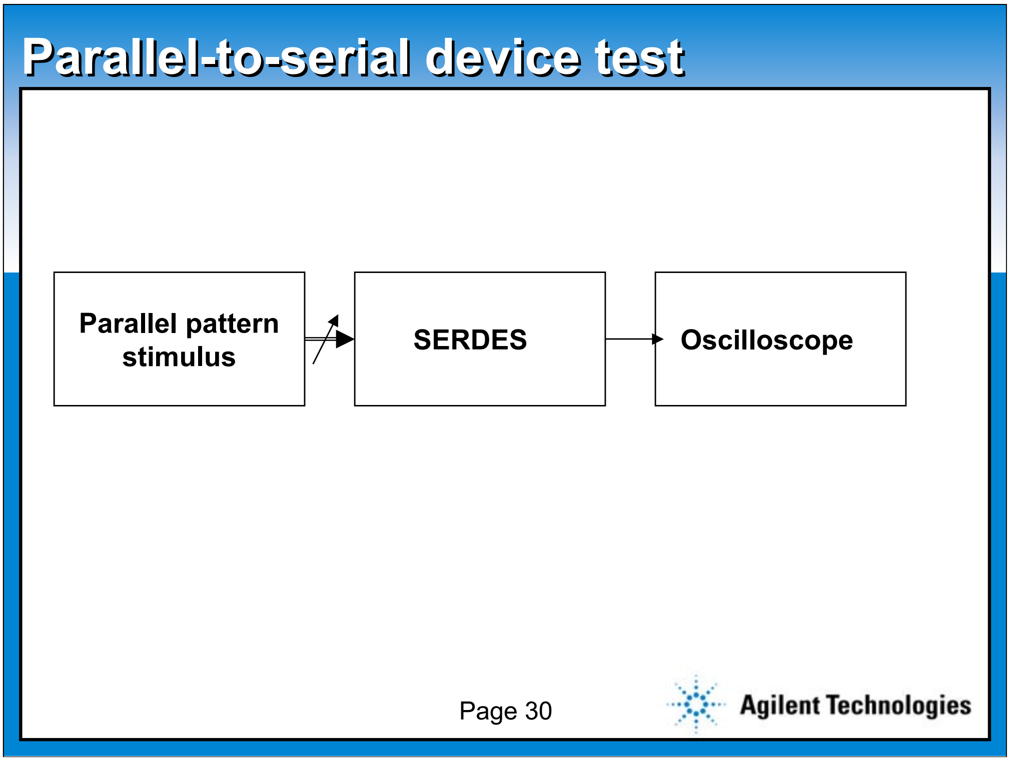
As I mentioned earlier, this instrument actually measures bit error rate, and can generate an eye diagram based on bit error rate. What the eye is showing here is that as we vary the sampling point in volts and time, the error rate changes. The colors in the eye represent iso contours of bit error rate.



Of course, you can also use this type of instrument as a parallel pattern stimulus to test devices such as a SERDES (serializer-deserializer). In this example, the generator is used to provide parallel pattern stimulus to the parallel side of a SERDES, while an oscilloscope is used to monitor the resulting eye on the serial side. We'll see another example of this when we get to the live circuit examples.

Autonomous circuit examples

- SPI-4.2
- 266 MT/s DDR memory

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Now we'll move to another class of measurements, in which the circuit under test is running on its own, not depending on stimulus. The two examples I'll show are an SPI-4.2 data bus, and a 266 Mtransfer/second DDR memory interface. In both of these examples, I'll introduce a revolutionary new feature called "eye scan," which allows a logic analyzer to acquire eye diagrams on many signals simultaneously.

SPI-4.2 example

This example uses SPI-4.2 signals, generated by the PMC-Sierra Xenon chip set.

SPI-4.2 is a standard used for chip-to-chip communications in high-speed routers.

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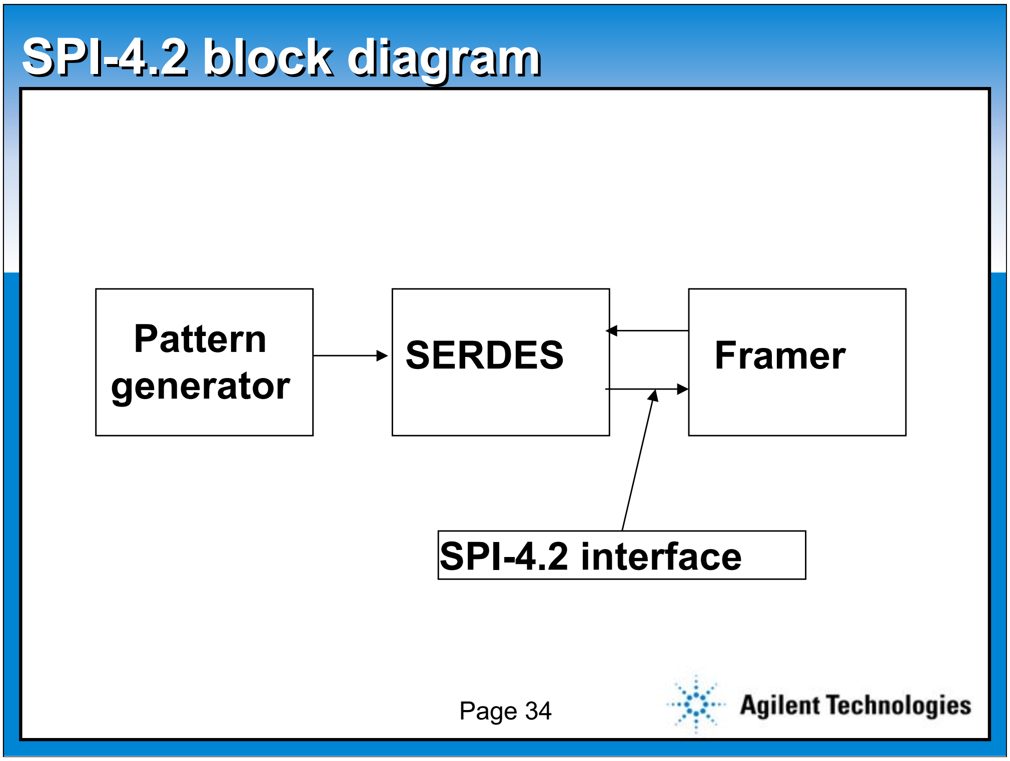
The first example is the SPI-4.2 interface. This is a chip-to-chip communication standard that is used for parallel data transfer in high-speed data communications hardware such as 10G Ethernet. The example I will use here is from PMC-Sierra and their Xenon chip set.

SPI-4.2 bus

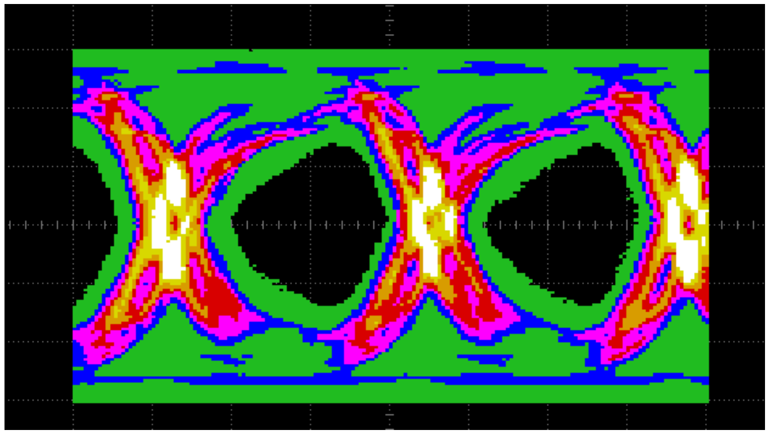
- LVDS signals
- Up to 840 Mtransfers/second
- 16 data bits + 1 frame bit

The SPI-4.2 bus uses LVDS (low voltage differential signalling). It operates at data rates up to 840 Mtransfers/second. One SPI-4.2 link includes 16 data signals and one frame bit, plus clock.

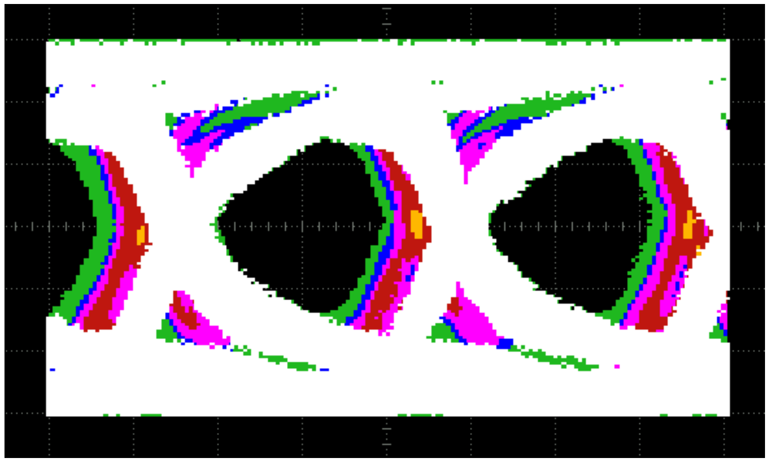


The example looks at signals passing over an SPI-4.2 interface operating at 622 MT/s between a framing chip and a SERDES chip. The stimulus was provided by a high-speed serial pattern generator.

SPI-4.2 eye



SPI-4.2 eye



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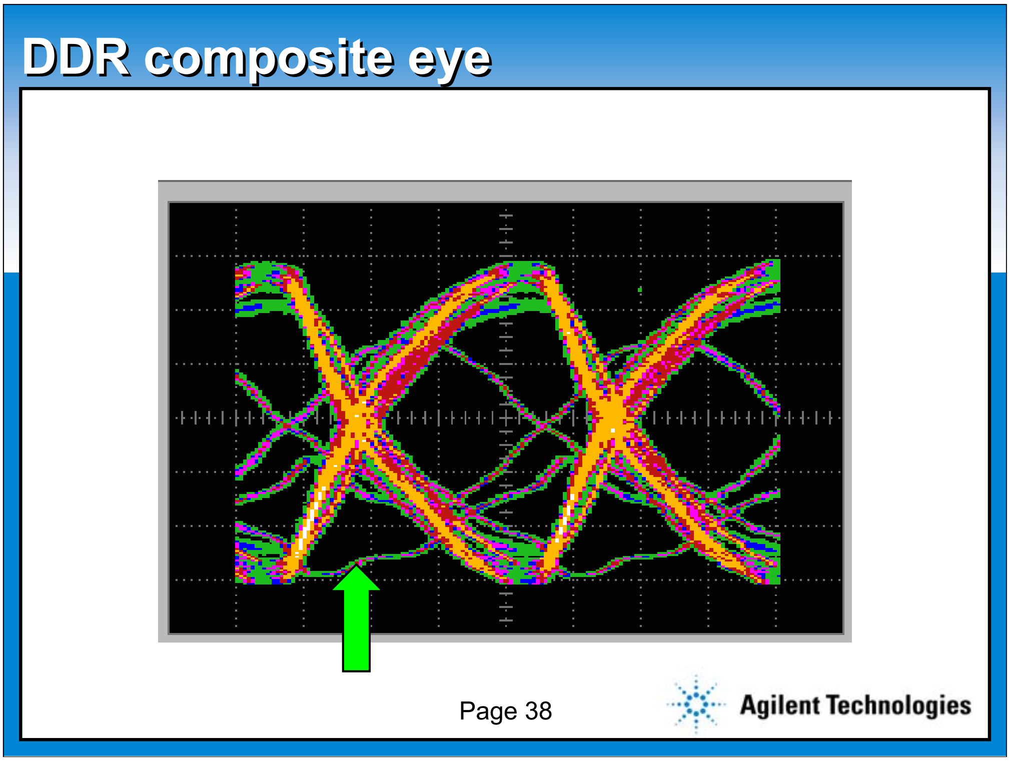
One of the unique features of the PMC-Sierra chip set is its ability to adaptively align the clock-to-data timing to account for skew, etc. The eye scan display shows all the 16 signals in the SPI-4.2 data group, so it is easy to see the timing relationship of all the eyes in one view. In this slide, one data signal is highlighted in white so we can more easily visualize its relationship to the composite of the other 15 data signals.

This example also shows how sometimes what we might think of as an autonomous circuit test also involves stimulus. By using a serial pattern generator, the designer was able to check out the timing with many different serial patterns, including PRBS and typical traffic.

DDR example

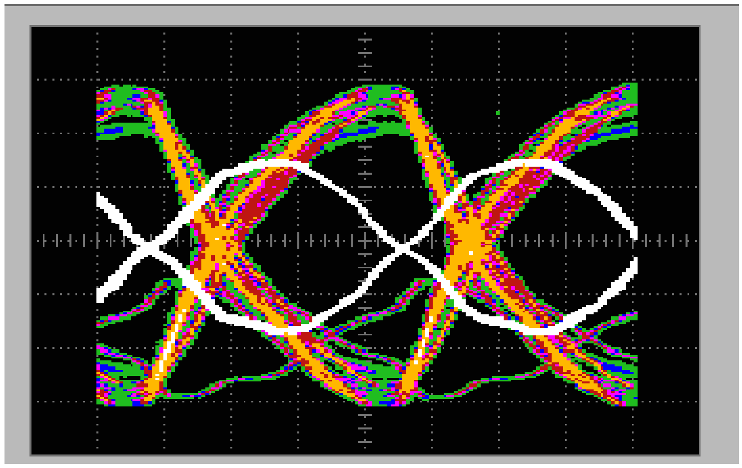
- 266 MT/s
- SSTLII levels
- 32 data bits
- 2 strobes
  - Read, write

The next example is a DDR (double-data-rate) memory bus. This one is operating at 266 Mtransfers/second. In each group There are 32 data bits and 2 strobes. Critical timing parameters include the overall eye opening and the timing between the strobe and the data eye.



Here we see the composite eye diagram of one lane of the data bus and the associated write strobe. Looks like something kind of strange going on with the compressed-looking signal toward the bottom of the graticule.

DDR highlighting write strobe



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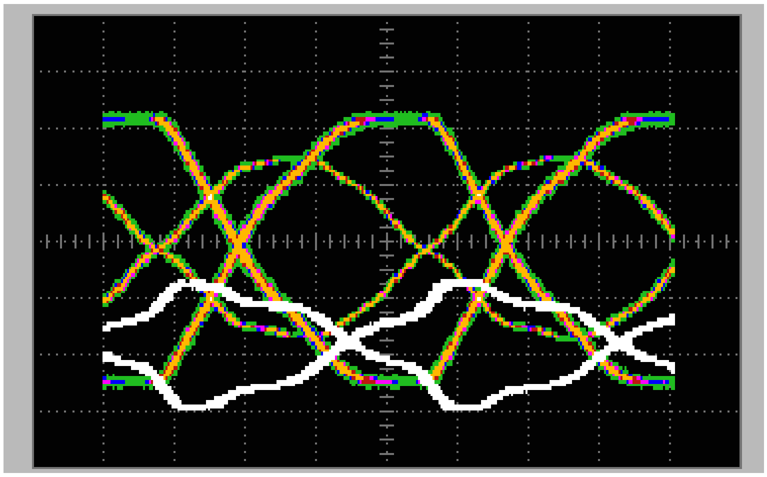
In this view, we've highlighted the write strobe in white, and we can see that it has the correct timing relationship to all the data bits.

DDR simultaneous switching noise



Here we've highlighted the problematic-looking signal in white. Turns out that signal was not supposed to be switching in this case. The system was running some test software that set it up so that bit should not be switching. As you can see, there is some noise being induced on it. Turns out that it was being corrupted by simultaneous switching noise.

Eye measurement tools

- Stimulus
  - Pulse generators
  - Parallel pattern generators
- Oscilloscopes
- Oscilloscope probes
- Eye scan
- Parallel pattern generators/analyzers

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Now let's move on to the next section of the eSeminar, where I'll discuss some of the tools you need to be successful with eye diagram measurements.

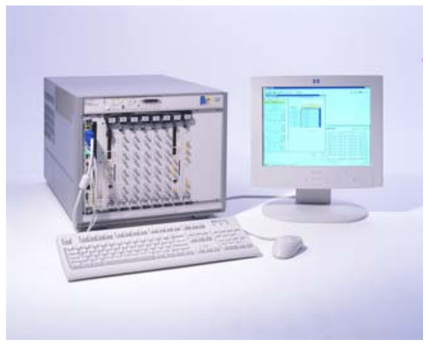
Pulse generators

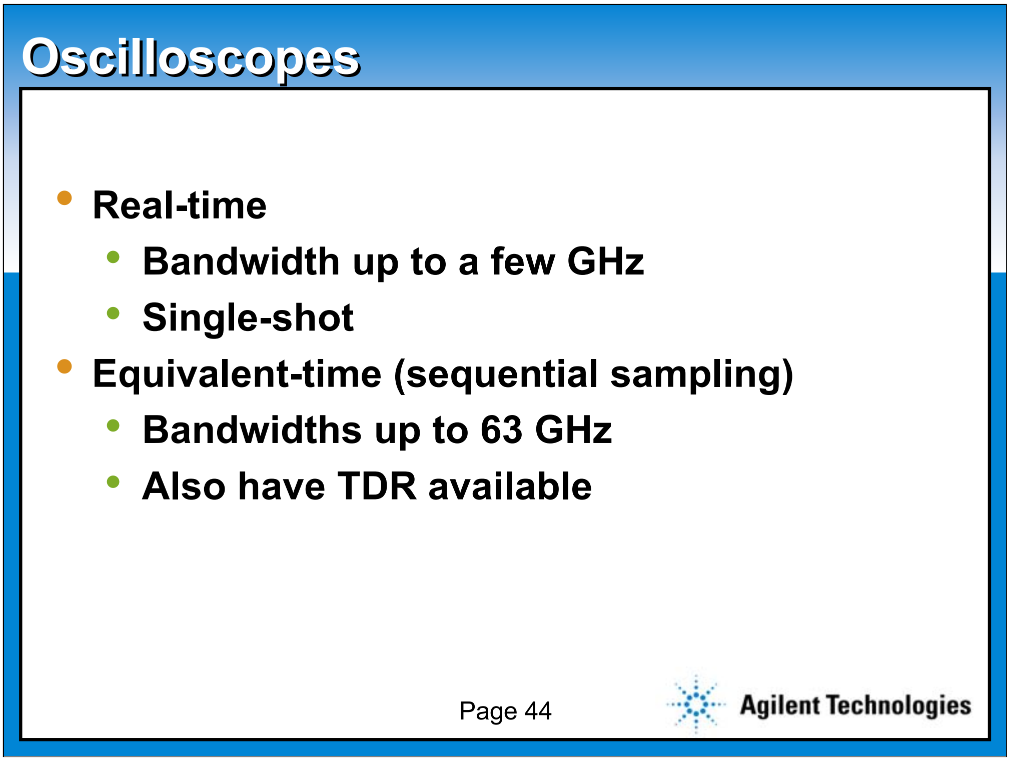
- Pulse flatness
- Time base stability
- Serial pattern generation, including PRBS
- Ability to add controlled jitter
- Ability to vary crossover

When selecting a pulse generator, be sure to consider pulse flatness and time base stability, as well as the ability to stress the device under test by adding controlled jitter and varying the crossover of differential signals. Serial pattern generation can also be very useful, particularly PRBS (pseudorandom binary sequence) generation. The longer the PRBS the better.

Parallel pattern generator/analyzer

- Look for ability to vary timing, amplitude
- Look for ability to measure bit error rate





There are two flavors of oscilloscopes: real-time and equivalent-time. Real-time scopes sample at a rate many times the signal's repetition rate, and acquire a complete waveform on each trigger event. They have the very useful benefit of capturing single-shot waveforms. This can be very handy when it comes to troubleshooting.

Equivalent-time scopes, sometimes called sequential sampling or repetitive sampling, typically have much higher bandwidth, up to 63 GHz. TDR instruments are typically plug-in modules for an equivalent-time scope, so you get two useful instruments for one investment. Equivalent-time scopes acquire one sample on each trigger event, so they don't have single-shot capability.

Oscilloscope eye measurements

- Eye height (V) and width (T)
- Mask testing
- Crossing %
- Q-factor
- Duty cycle distortion
- Extinction ratio

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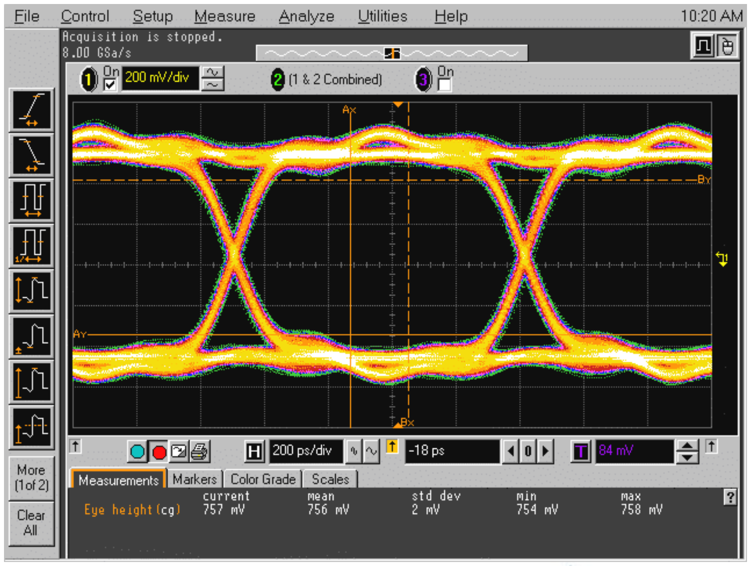
Here are some of the common measurements available in oscilloscopes for examining eye diagrams.

I'll show a few examples in following slides.

Eye height



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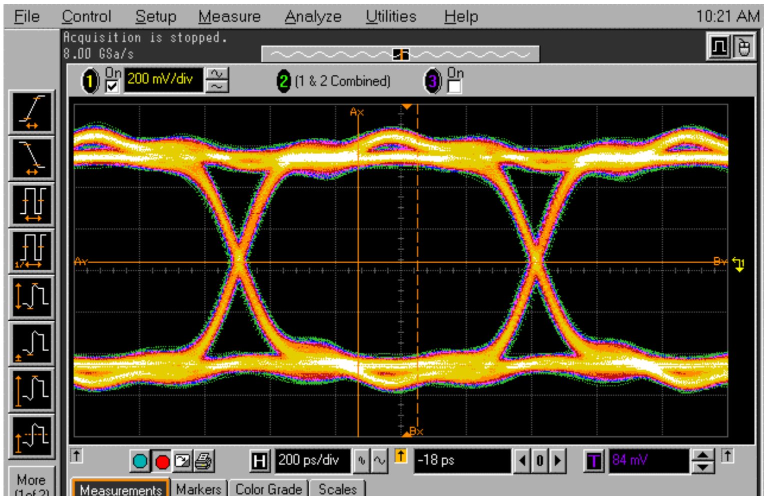
Eye crossing percent



	current	mean	std dev	min	max
Eye height (cg)	757 mV	756 mV	2 mV	754 mV	758 mV
Eye width (cg)	851.7 ps	851.7 ps	0.0 s	851.7 ps	851.7 ps
Crossing % (cg)	50.6%	50.6%	0.0%	50.6%	50.6%

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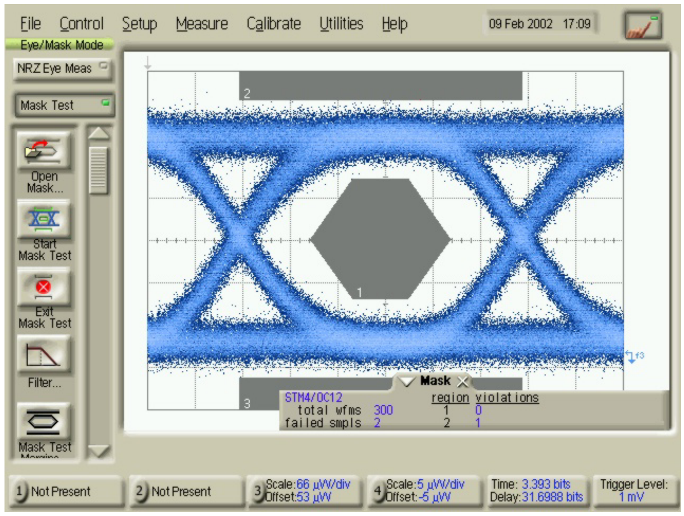
Mask test example



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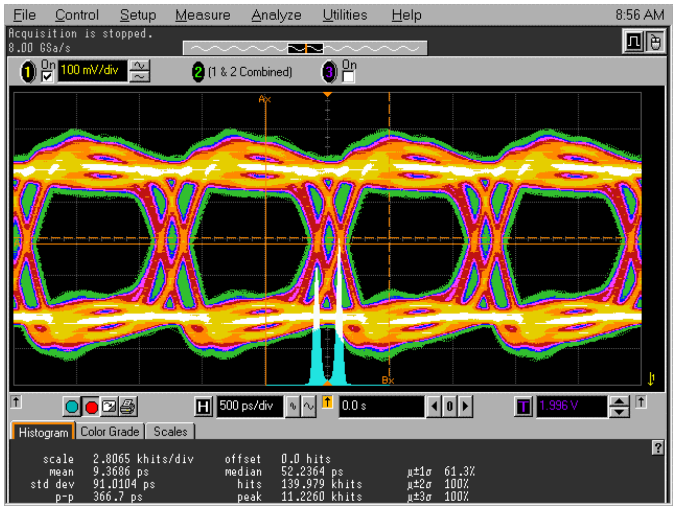
Scope histogram



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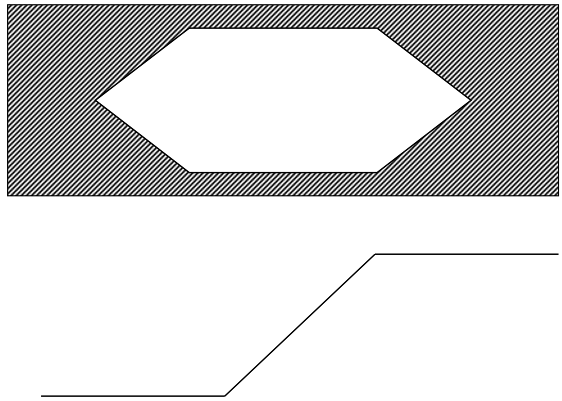
Here, for example, is a histogram measurement. The histogram gives you some statistical insight into the eye.

Notes on scopes and eyes

- Trigger threshold relationship to logic threshold
- Rising or falling clock only
- Throughput is important

Trigger threshold



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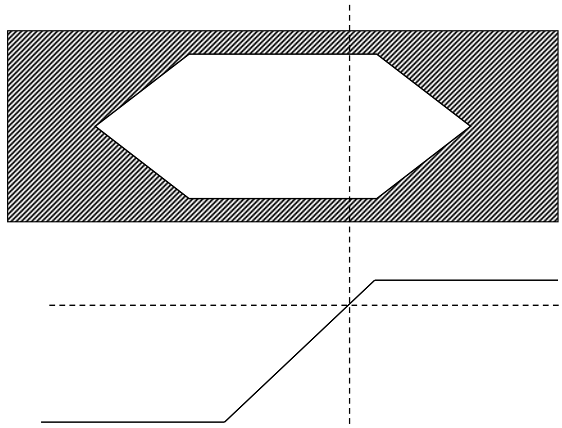
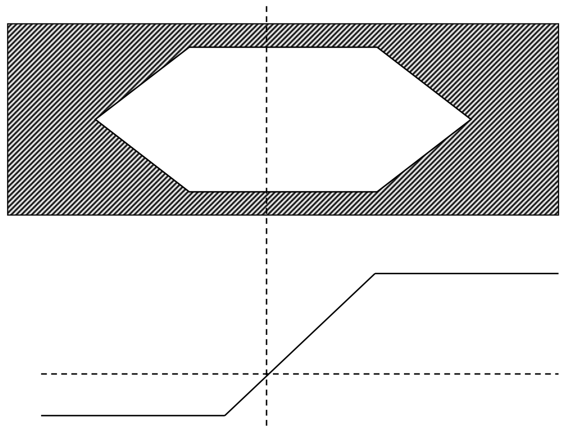
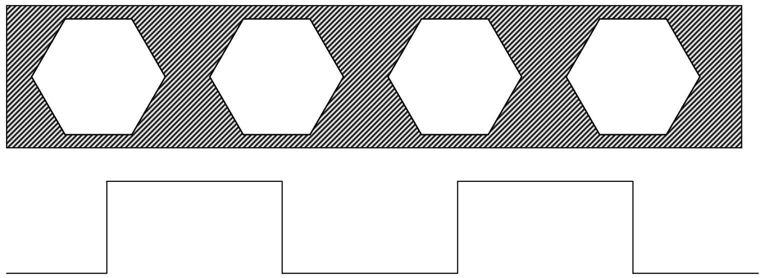
Trigger threshold



Trigger threshold



DDR dilemma



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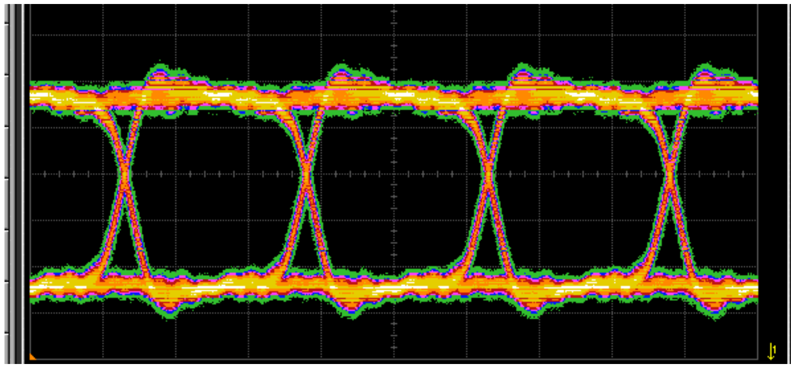
DDR eye on a scope



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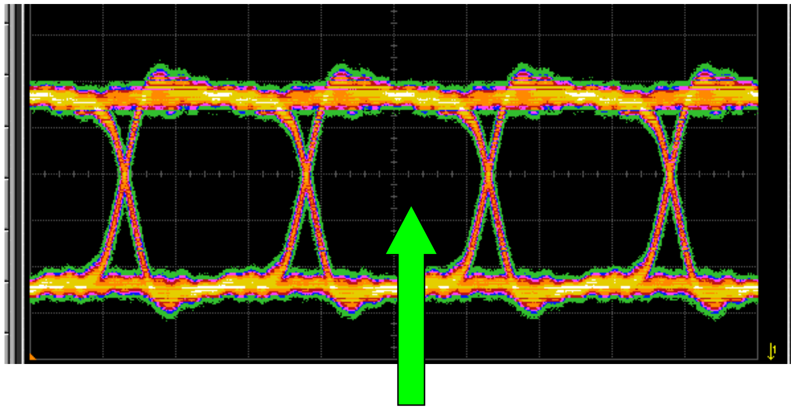
DDR eye on a scope



Eye corresponding to rising edge of clock

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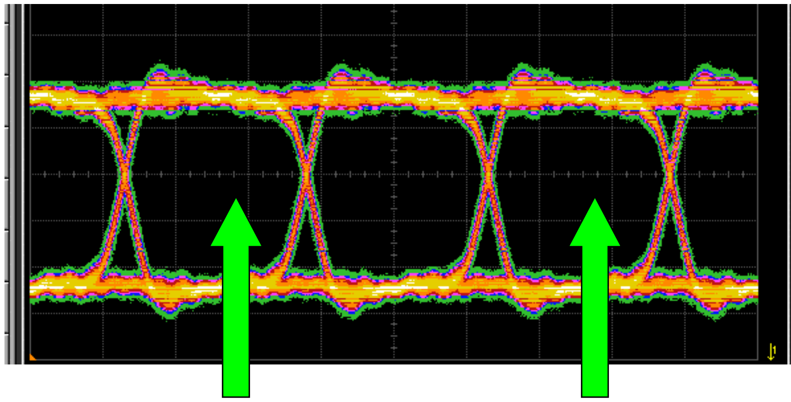
DDR eye on a scope



Eyes corresponding to falling edge of clock

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Oscilloscope probes are critical

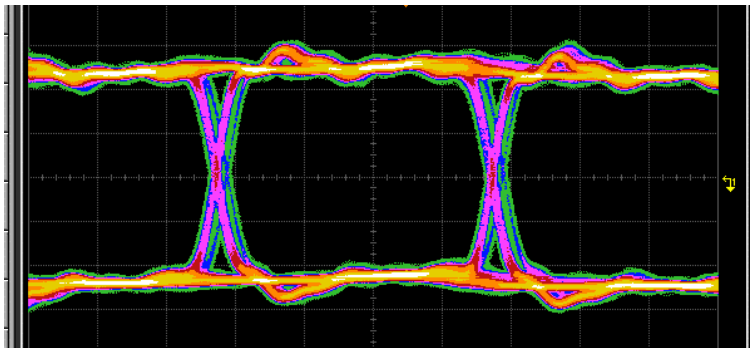
- **The measurement can't be any better than the probe**
- **The methods used to connect the probe are usually the limiting factor**

I can't stress enough how important probes are to scope measurements. And even with a great probe, you have to think about the accessories you use to connect it to your circuit. The probe becomes a part of the circuit under test as soon as you hook it up. The signals you're measuring have to pass through the probe and any accessories you use before the scope can see them. You'd be amazed how many Petahertz of scope bandwidth are wasted every day by putting 3-inch-long wires on the front of scope probes.

Probing examples

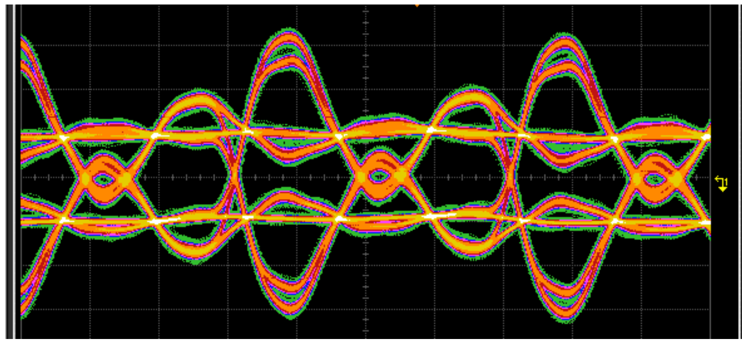
- All with 500 MHz PRBS
- Best-case probe
- 1 inch wire in series with probe

Probing comparison



Probe

Probing comparison



Probe + 1 inch wire

Eye scan

- Examine eye on an entire bus
- Save time and increase confidence
- Part of the Agilent 16760A logic analyzer
- Very fast view of all signals
- View signals in context

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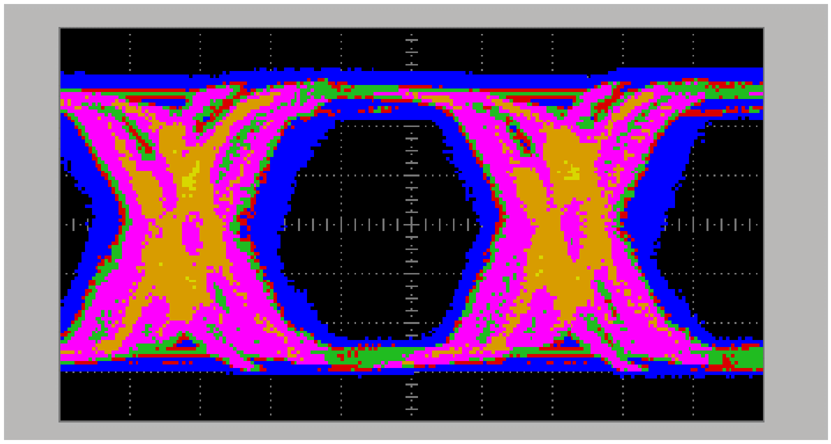
In the two examples I referred to “eye scan.” This is a feature of Agilent’s 16760A logic analyzer that allows you to examine the eye diagrams on an entire bus. This can save you significant time when you’re dealing with a lot of signals on several buses. You can use that time to the beach, or to gain confidence by looking at more eye diagrams under more conditions. Maybe a little of both is the correct work-life balance. Until your boss catches on, that is. I’ll spend a little bit of time on this because it may be new to you.

The eye scan display



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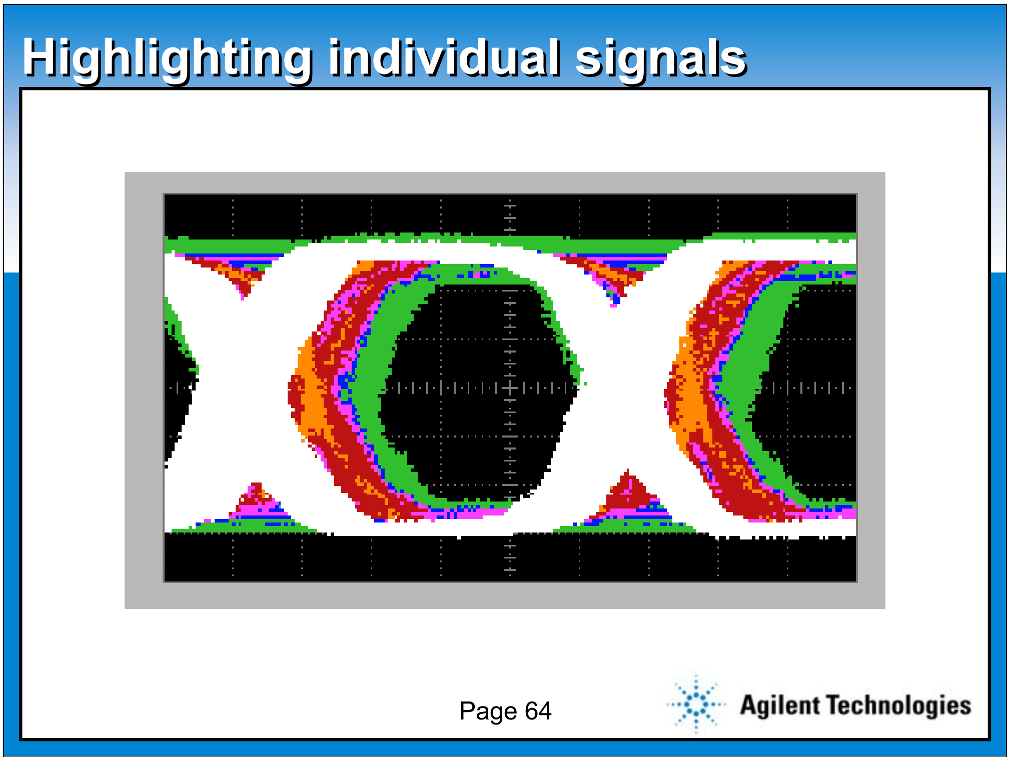
The eye scan display looks very similar to an eye diagram on an oscilloscope in color-graded persistence mode. Like a scope, the vertical axis is voltage, the horizontal axis is time.

Note that the “zero” time coordinate on the screen corresponds to the active clock edge. To compare to an oscilloscope, when you use an oscilloscope to measure an eye diagram, you trigger on the clock, which is connected to one of the scope channels. Clock transitions thus define the time=zero point on the scope display. The only difference in eye scan is that you don’t see the clock signal on the screen.



Individual signals can be highlighted, as we saw in the examples earlier. You can also view individual channels by themselves.

Comparing eye scan and scope

Eye scan

- Up to 169 signals per clock domain simultaneously
- Instant connection, if connectors installed
- Eye diagrams only
- DDR eyes
- Limited time and voltage range

Scope

- Waveforms or eye diagrams
- Rising or falling clock only
- Wide voltage and time range
- General-purpose

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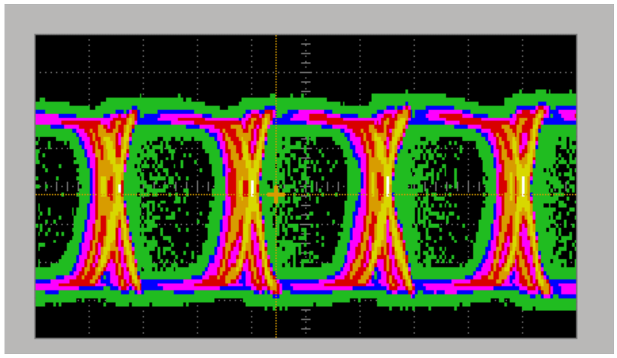
How does eye scan compare to an oscilloscope?

Eye scan can be used to view literally hundreds of signals with one press of the “run” button. And if you’ve designed the mass connectors for the logic analyzer into your board, connection is mighty fast. With a scope, you can typically look at 3 signals at a time, plus clock. A lot of the time spent with a scope is moving the probes around. One of our customers referred to signal integrity validation with the scope as the “probing sweatshop.” Eye scan can help you use your scope more effectively by showing you where to look with the scope. If all the signals look fine with eye scan, you’re done, and you can go on to the next test. If not, you can get out the scope and start chasing down the few that don’t look good.

You’ll still need your scope, by the way. Once you’ve found a problem signal, you may want to look at the actual waveform to see why it’s causing problems. Eye scan only shows you eyes, not waveforms.

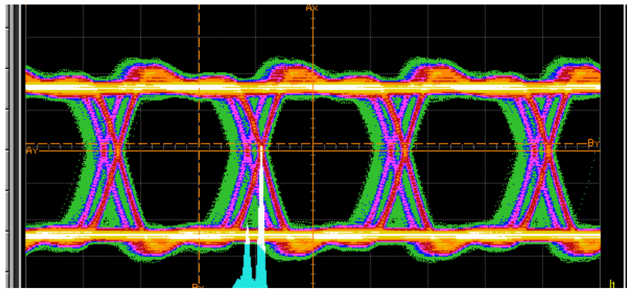
Finding infrequent violations



Noisy 800 MT/s PRBS signal

Eye scan after 5 minutes

Finding infrequent violations



Same signal

Oscilloscope after 5 minutes

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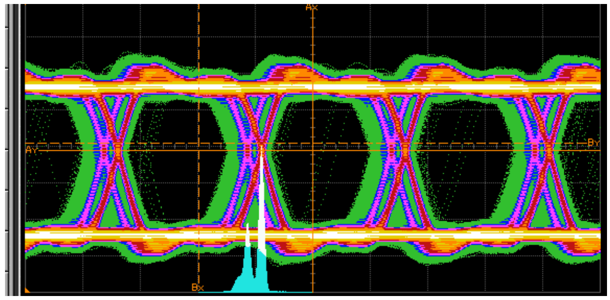
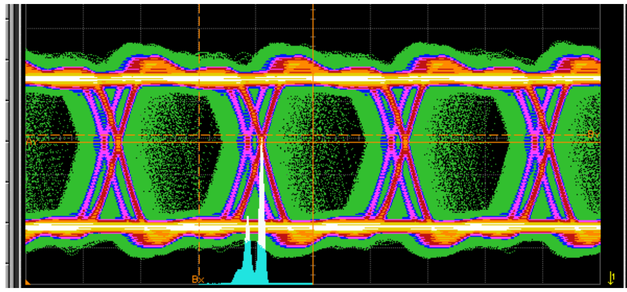
Finding infrequent violations



Same signal

Oscilloscope after 2 hours

Finding infrequent violations



Same signal

Oscilloscope after 72 hours

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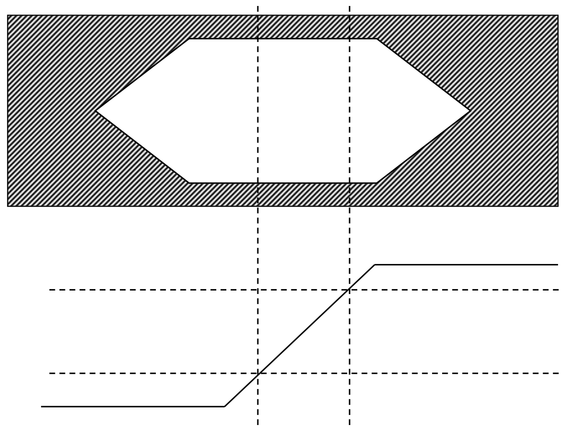
Throughput comparison

- Scope paints complete waveform on each trigger
- But it doesn’t trigger on every clock edge
- Your circuit responds to every clock edge

Throughput comparison

- Eye scan captures data at one V/T coordinate on each of many successive clock edges
- But it's only looking at one V/T coordinate at a time.

Clock threshold



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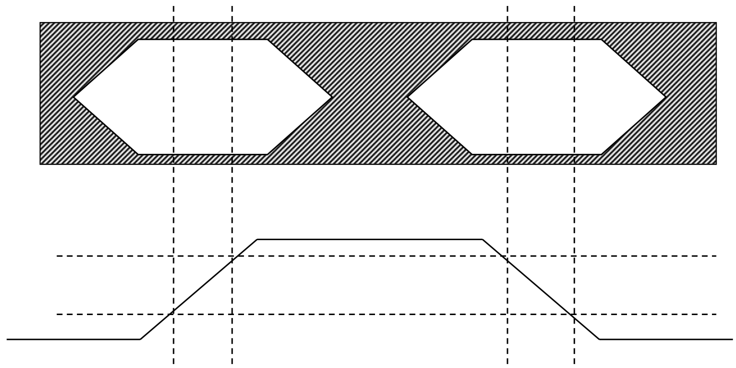
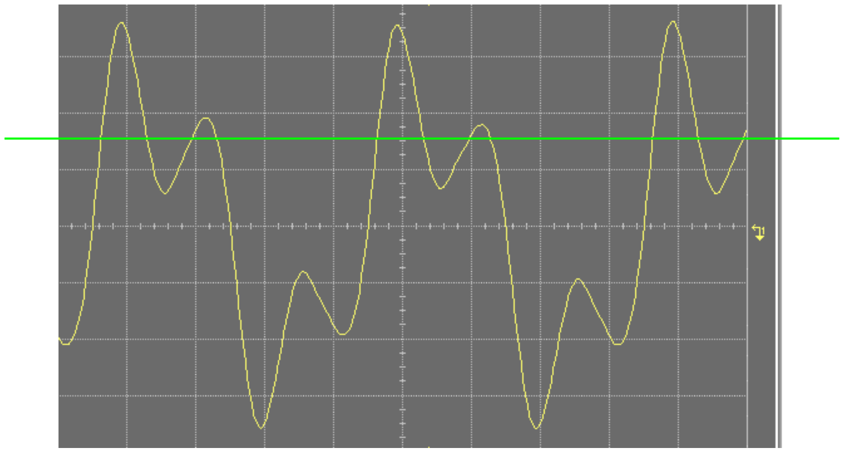
Clock threshold on DDR data



Impact of distorted clock



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Design phase tools

The following design tools were used in the examples in this NetSeminar

- Agilent ADS2002
  http://eesof.tm.agilent.com/products/
- TDASystems iConnect
  http://www.tdasystems.com
- atSpeed Oculus
  http://www.atspeed.net

Resources

- Article
- Application notes

Article

500-Mb/s Nonprecharged Data Bus for High-Speed DRAMs

Miyoshi Saito et al

IEEE Journal of Solid-state Circuits

Vol. 33, #11, Nov 1998

The literature on eye measurements is very sparse. The few papers that actually tackle the subject from a theoretical and/or mathematical viewpoint are so dense as to be unusable in practice. I like this particular article because it starts off with a really simple, graphical analysis of intersymbol interference, and it shows a practical example, all worked out, of how to analyze signal integrity.

Application notes

- **Measuring Extinction Ratio of Optical Transmitters, Agilent application note 1550-8**
  http://www.agilent.com/cm/rdmfg/appnotes/5966_4316e.shtml
- **Saving Time with Multiple-channel Signal Integrity Measurements, Agilent application note 1382-8**
  http://cp.literature.agilent.com/litweb/pdf/5988-5409EN.pdf

Application notes continued

- **Optimizing oscilloscope measurement accuracy on high-performance systems with Agilent active probes, application note 1385**
  http://literature.agilent.com/litweb/pdf/5988-5021EN.pdf
- **Agilent 86100A Infiniium High Bandwidth Oscilloscope demo guide, publication number 5980-2221E**
  http://literature.agilent.com/litweb/pdf/5980-2221E.pdf

Recap

- Use eye measurements starting in the design phase
- Stress your design in validation
- Pay close attention to instruments and measurement techniques, especially probing

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Desired outcome

May all your projects finish ahead of schedule, under budget, and exceed all performance and reliability goals.

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Now I'll turn it over to Gary.